REMARKS

Claims 1-7 are pending. By this response, claims 1 and 4 have been amended. Reconsideration and allowance in view of the below comments are respectfully requested.

Claims 1-6 stand rejected under 35 U.S.C. §103(a) in view of Maenaka et al. (US 7.039,254) and Jiang (US 7,242,819) and claim 7 stands rejected under 35 U.S.C. §103(a) in view of Maenaka, Jiang, and Utagawa (US 6,563,538). These rejections are respectfully traversed.

Claims 1 and 7 recite, *inter alia*, a plurality of interpolation circuits, each interpolation circuit independently calculating interpolation candidate data of the same interpolation pixel based on calculations performed on test interpolation data of a plurality of normal pixels neighboring the interpolation pixel, where each interpolation circuit uses a different interpolation method; wherein said test interpolation data is calculated for each of said normal pixels on the assumption that said normal pixels are lost using said different interpolation method; a determining circuit for selecting one of the interpolation circuits based on a difference between the test interpolation data and actual pixel data of said plurality of normal pixels. Claim 4 recites similar features. Applicants respectfully submit that the combination of Maenaka and Jiang fail to teach or suggest these claimed features.

In the embodiments of the present invention as recited in claims 1, 4 and 7, a plurality of interpolation circuits each using a different technique performed independently and interpolation calculation on the same normal pixel and obtains test interpolation data. Thus, the actual data value of the normal pixel is known and the interpolation result (test interpolation data) of the normal pixel is also known. By comparing these two data the interpolation circuit that performs the best can be determined and then selected to obtain the actual interpolation pixel (missing pixel) located in the image data.

Maenaka does not teach these features. Maenaka teaches various interpolation methods. Each interpolation method is a different embodiment of Maenaka. These different methods are not integrated as part of a determination of the best method to use for interpolation. Further, there is no teaching in Maenaka of using normal pixels to determine what its interpolated data would be if it was a missing pixel and then comparing this data to its actual pixel data.

Thus, Maenaka fails to teach the claimed features recited in claim 1 for which it is provided to teach.

Futher, Jiang fails to remedy the deficiencies of Maenaka. Jiang teaches an edge direction interpolation block (FIG. 8) where various summing, division blocks and multiplexer are used to determine the output signal X. The luminance values of various pixels are added using the summing blocks. The sums are then divided by the division blocks and multiplexed by the multiplexer. See Col. 13, lines 32-67. The use of this interpolation block and its various summation blocks, division blocks and multiplexer is implemented in a single method. The use of the adders, dividers and multiplexer is not to implement different interpolation methods but instead to implement a single method taught in Jiang.

Thus, Jiang fails to teach the current features for which it is provided to teach and furthermore, fails to remedy the deficiencies of Maenaka. Also, Utagawa fails to remedy the deficiencies of Maenaka and Jiang.

Therefore, in view of the above, it is respectfully submitted that claims 1, 4 and 7 are distinguished from the cited art. Dependent claims 2, 3, 5 and 6 are likewise distinguished from the cited art for at least the reasons above as well as for the additional features they recite. Accordingly, reconsideration and withdrawal of the rejections are respectfully requested.

Conclusion

For at least the above reasons Applicants respectfully submit Claims 1-7 are distinguishable over the cited art. Favorable consideration and prompt allowance are earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Chad J. Billings Reg. No. 48,917 at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

Dated: November 13, 2009

Respectfully submitted,

By _____

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